ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory device having a small layout size includes a memory cell array in which a plurality of memory cells are arranged in a row direction and a column direction. The memory cell array includes a plurality of element isolation regions. Each of the memory cells includes a source region, a drain region, a channel region located between the source region and the drain region, a select gate and a word gate disposed to face the channel region, and a nonvolatile memory element formed between the word gate and the channel region. A wordline connection section which connects at least one of a plurality of word gate interconnects in an upper layer with at least one of the word gates is disposed over at least one of the element isolation regions.